

09/816,338

Proposed Amendment to Claim 9

Draft Claim 9

9. (Amended) A semiconductor testing apparatus comprising:
a pattern memory which stores pattern generating instructions for testing a semiconductor device;
a sequence control circuit according to claim 1 which supplies said an instruction memory address to said pattern memory in order to control the output sequence of the pattern generating instructions that are read out from said pattern memory;
a pattern generating circuit which generates test patterns supplied to said semiconductor device and expectation patterns in accordance with said pattern generating instructions that are output from said pattern memory; and
a determination circuit which determines the quality of said semiconductor device based on said expectation patterns and signals that are sent from said semiconductor device in accordance with said test patterns;
wherein said sequence control circuit comprises:
a program counter control section which decodes a sequence control instruction that is executed in the n-th cycle to output a program counter signal in the (n+1)th cycle as said instruction memory address for specifying a sequence control instruction that will be executed in the (n+1)th cycle; and
an instruction memory section which outputs said sequence control instruction executed in the (n+1)th cycle to said program counter control section in the (n+1)th cycle based on a program counter signal for specifying said sequence control instruction that is executed in the n-th cycle.

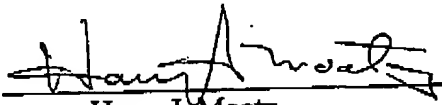
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Expires: August 27, 2004



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